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# Design of low power Universal Shift Register Using Pipe Logic flip flops

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**Abstract**: Power consumption and area are the important parameters to be considered for designing low power applications. This paper proposes the design of low power universal shift register using pipe logic. Since flip flops are an inherent building block in universal shift register, various flip flops are surveyed and implemented in PIPO shift register. Flip flop using pipe logic is considered based on the comparison of power and area. Finally, a low power universal shift register is designed using pipe logic. The proposed USR is simulated with different clock frequencies ranging from 100 MHz to 500MHz. Simulation of these flip flops and the universal shift register is done using Tanner tool at 180nm technology. Further, the average power and the PDP are improved by 33% and 27% when compared with existing design respectively. So the proposed design is suitable for low power and high performance applications.

**Keywords**: Flip-flops, Shift register, power, delay, PDP.

## I. INTRODUCTION

The developing significance of portable systems and the need to limit power consumption in Very Large Scale Integration (VLSI) chips have led to massive and innovative developments in low-power design during these recent years. Designers are striving for small silicon area, speed, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. A large proportion of digital circuits are designed to be synchronous circuits in order to reduce the complexity of circuit design. Flip-flops are the critical timing elements in digital circuits which have a large impact on the circuit speed, area and power consumption. Flip-Flop is an electronic circuit that is used to store a logical state of any data input signals with response to the clock pulse.

D-type flip-flops (DFF's) contribute a significant part of the total power dissipation of the system and it is one of the most fundamental building blocks in VLSI systems. It captures the value of D-input at a definite portion of clock cycle. The captured value becomes the Q output. These flip-flops are an essential part of many electronic devices very, as they form the basis for shift registers, which. The advantage of the D flip-flop when compared with D-type transparent latch is that the signal on the D input pin is captured at the moment when the flip-flop is clocked and changes on the D input will be ignored until the next clock event.

In this paper some flip-flops are being surveyed in the literature such as double edge triggered flip-flop (DETFF), Conditional data mapping flip-flop (CDMFF), clocked pair shared flip-flop (CPSFF), CPSFF using MTCMOS, Single-ended Conditional Capturing Energy Recovery (SCCER), flip-flop using PIPE logic. These surveyed flip-flops are implemented in PIPO shift register. Based on the value of power obtained the best two among the flip-flops are selected and the Universal shift register is designed using those flip-flops.

This paper is structured as follows: Section I provides the introduction to various flip flops. Survey of various flip-flops is explained in section II. Section III explains the design of flip-flops using modified pipe logic. Section IV explains the implementation of flip-flops in PIPO shift register. Section V explains the design of universal shift register. Results and performance for newly proposed designs are compared in terms of average power, delay and PDP in Section VI. Paper ends with the conclusion in Section VII.

## II. LITERATURE SURVEY

In this paper, we survey various D flip-flops namely double edge triggered flip-flop (DETFF), Conditional data mapping flip-flop (CDMFF), clocked pair shared flip-flop (CPSFF), CPSFF using MTCMOS, Single-ended Conditional Capturing Energy Recovery (SCCER).

### *A.* Double Edge Triggered Flip-Flop

The DET flip-flop is basically a Master Slave flip-flop structure. This has two data paths. This flip-flop uses six N-type clocked pass transistors and works on positive edge. The upper data path is triggered on the rising edge and lower data path is triggered on falling edge. The data paths have feedback loops connected such that the logic level at the output is recalled whenever the clock is stopped. The operation of this flip-flop is such that when the data value is high, inverter switches the signal to low, which will make the transistor pull high. The inverter switches the signal from low to high which will isolate the data from VDD and keep the value low until the data value is low. The schematic of DETFF is shown in Fig.1.

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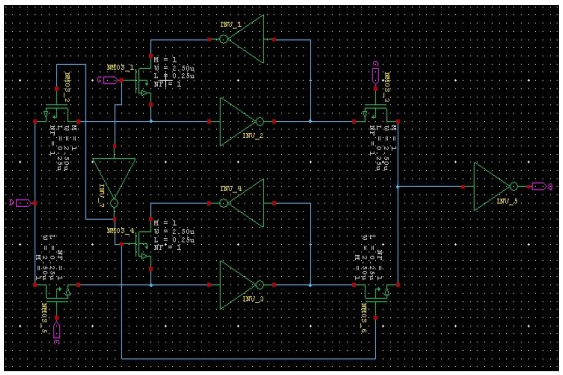

Fig.1. Double Edge Triggered Flip-Flop

*B.* Single-Ended Conditional Capturing Energy Recovery Flip-Flop (SCCER)

SCCER is a pulsed flip-flop. It is an energy recovery flip-flops that work effectively for a single-edge of a sinusoidal clock. The term 'Conditional capturing' is used to minimize flip-flop power at low data switching activities by eliminating redundant internal transitions. The PMOS transistors are used for SET and RESET. The operation of the flip-flop is that the transistor MN3 controlled by the output QB, provides conditional capturing. The discharge path contains two NMOS transistors N1 and N2 connected in series. In order to eliminate the node switching, N3 is employed. When data remains high, N3 is controlled by Q feedback and no discharge occurs. The schematic of SCCER is shown in Fig.2.

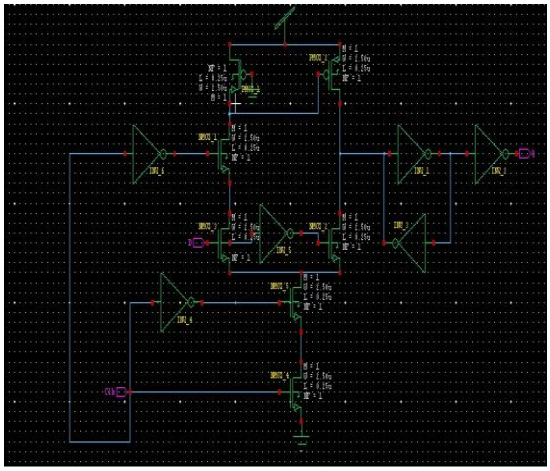

Fig.2 Single-Ended Conditional Capturing Energy

Recovery Flip-Flop

*C.* Clocked Pair Shared Flip-Flop (CPSFF)

CPSFF uses 4 clocked transistors. In this flip-flop the clocked pair is shared by the first and second stage. The first stage is mainly for the LOW to HIGH transition, while the second stage being responsible for HIGH to LOW transition. Removal of extra switching activity takes place by controlling the discharge path when the input is at stable level '1'.

Controlling of the discharge path results by adding NMOS, this is controlled by Qb. As long as input remains at stable level '1', the discharge path of the first stage helps in preventing evaluation in the approaching clock cycles. Since the PMOS is always ON in CPSFF, it allows the internal node to be always connected to Vdd, thus prevents the floating problem. The schematic of CPSFF is shown in Fig.3.

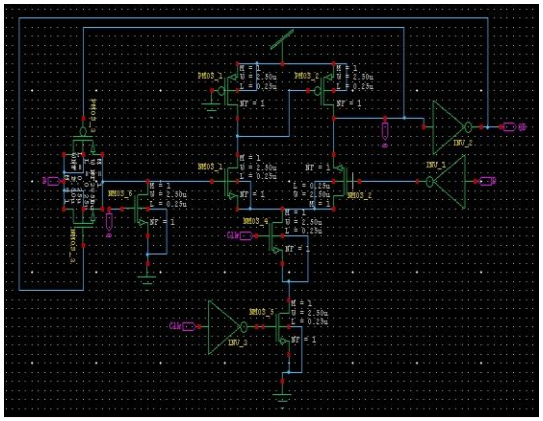

Fig.3 Clocked Pair Shared Flip-Flop (CPSFF)

*D.* Conditional Data Mapping Flip-Flop (CDMFF)

CDMFF uses 7 clocked transistors .A conditional data mapping is deployed in the circuit to map the inputs by using outputs as control signals. The operation of this flip-flop is such that when the data remains '0' or '1', the pre-charging transistors P1 and P2 keep switching which results in redundant clocking. When the CLK transits from 0 to 1, CLKDB will have a value '1' and will be in evaluation mode. If D is '1', the pull down network will be detached by N3 using data mapping method. If D is '0', the pull down network will be detached from GND. The schematic of CDMFF is shown in Fig. 4.

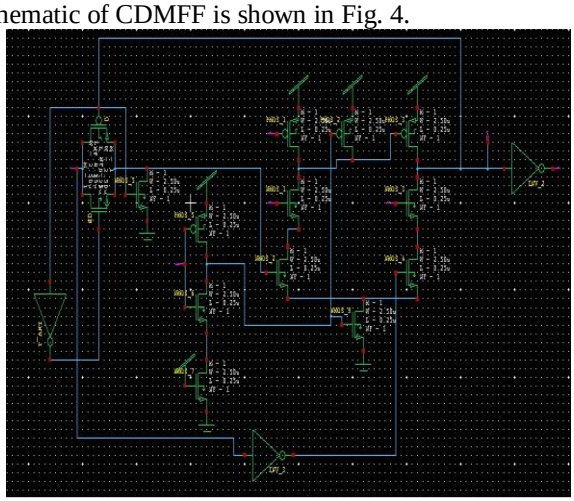

Fig.4 Conditional Data Mapping Flip-Flop (CDMFF)

*E.* CPSFF Using Multi-Threshold Voltage CMOS (MTCMOS)

Multi-Threshold Voltage CMOS (MTCMOS) is one among the highly known circuit technique to reduce the leakage current. The circuit works on two operational modes, one being the active and other being the sleep mode for efficient power controlling in MTCMOS technology. To reduce standby leakage power consumption and to ensure efficient implementation of


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sequential elements, the clocked pair shared flip-flop using MTCMOS technique is used. When both clk and clkdb are at logic '1', the flip flop works. The NMOS M3 is controlled by a feedback signal. For input D=1and S=1, Q will be high, switching ON the transistor M8, and turning OFF M3. The output Q is pulled up by PMOS M2 whereas M4 is used to pull down Q when D transits to 1.When D=0 and Y=1 at the arrival of clock pulse. When the input D transits from 0-1 the short-circuit occurs when M1 is always ON, thus disconnecting the discharge path and turning off M3 after two gates delay by feedback signal. Even if the input D stays high as M3 disconnects the discharge path, there will be no short-circuiting. The output of the flip flop depends upon the state previously acquired by Q and QB along with the clock and the data signal inputs provided. The schematic of CPSFF USING MTCMOS is shown in Fig.5.

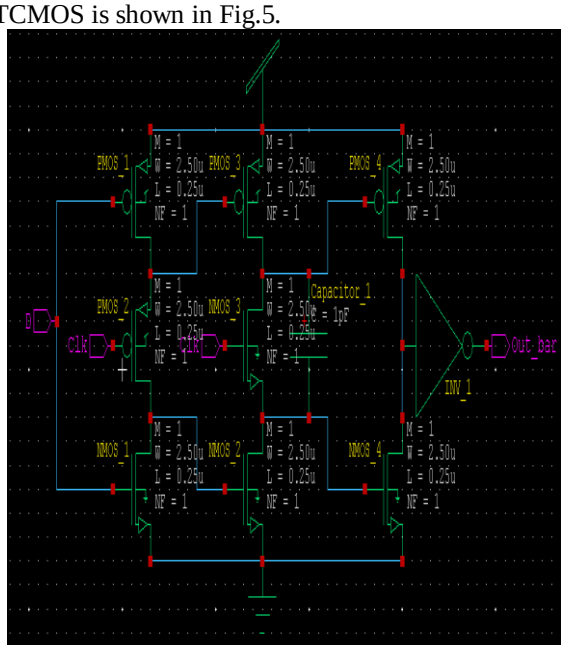


Fig.5 CPSFF Using Multi-Threshold Voltage CMOS

## III. DESIGN OF FLIP-FLOP USING MODIFIED PIPE LOGIC

The operation of this flip flop is such that the first stage becomes a regular inverter, when the clk is low. Then, D1H = D1L = DB. Apart from the first stage the last stage is also an inverter, so assume that D2H = D2L = Q. The second clocking transistor split these two stages which are divided by an inverter. Suppose D ≠ Q, so that D1H = D1L = D2H = D2L, but it will not be possible if the split inverter were a regular inverter. D2H affects a transistor in the final stage which turns on only when provided with a low gate voltage whereas the upper half of the split inverter can only pull D2H to a high level.

D2L affects a transistor which turns on only in response to a high gate voltage. Conversely, the other lower half of the split inverter can only pull D2L to a lower level. The first half of the circuit behaves like a normal inverter and the value of D propagates a step to the right whereas when the clock toggles, a similar operation takes place in the left half of the circuit. The schematic of flip-flop using pipe logic is shown in Fig.6.

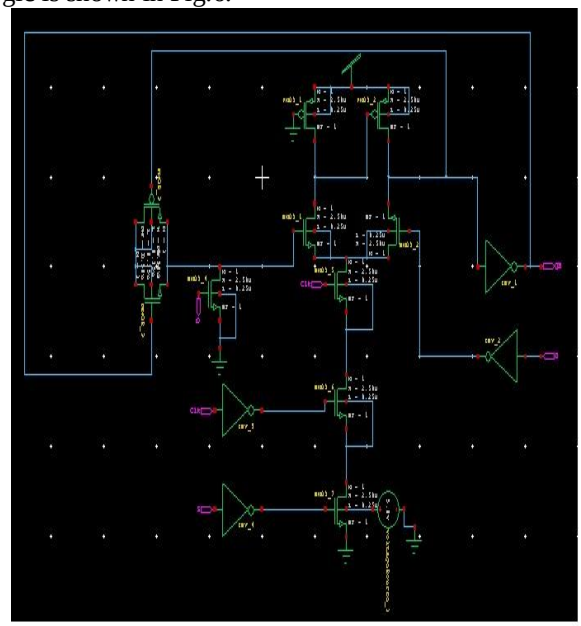

Fig.6 Design of Flip-Flop Using modified Pipe Logic

## IV. IMPLEMENTATION OF FLIP FLOP IN PIPO SHIFT REGISTER

Various parameters have been measured for the flip flops in above surveyed flip flops. Based on those parameters two flip flops namely DETFF and flip flop using PIPE logic are considered and those flip flops are implemented in PIPO shift registers. The operation of PIPO shift register is that the parallel data is loaded simultaneously into the register, and shifted to their respective outputs by the same clock pulse hence we apply four bit of data to a parallel-in and parallel-out shift register at $D_A$ $D_B$ $D_C$ $D_D$. The mode control, which may be multiple inputs, controls parallel loading vs. shifting. The data will be shifted one bit position for each clock pulse. The shifted data will be obtained at the outputs $Q_A$, $Q_B$, $Q_C$ and $Q_D$. The "data in" and "data out" are used for cascading multiple stages. But we can only cascade data for right shifting. By adding a pair of left pointing signals, "data in" and "data out", the cascading of left-shift data is performed. The design of PIPO shift register using DETFF and flip flop using PIPE logic is shown below in Fig.7 and Fig.8.

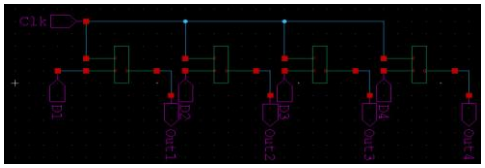


Fig.7 Design of PIPO shift registers Using DETFF

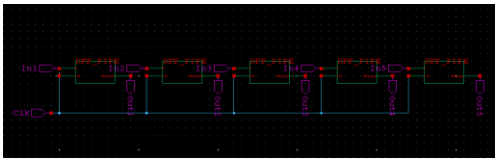

Fig.8 Design of PIPO shift registers Using PIPE logic


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## V. DESIGN OF UNIVERSAL SHIFT REGISTER

A universal shift register is a logic circuit that can transfer data in three different modes. Similar to a parallel register it can load and transmit data simultaneously. Like shift registers it can also load and transmit data in serial fashions through left or right shifts. In addition, the universal shift register combine the capabilities of both parallel and shift registers. On a particular job, a universal register can load data in series and then transmit output data in Parallel. Universal shift registers are also used in computers as memory elements. The different modes of operation in universal shift register in the block diagram are shown as follows.

TABLE I: OPERATING MODES OF UNIVERSAL SHIFT REGISTER

| OPREATING MODE | S1 | S0 |
|---|---|---|
| Locked | 0 | 0 |
| Shift right | 0 | 1 |
| Shift left | 1 | 0 |
| Parallel loading | 1 | 1 |

When S1=0 and S0=0, the shift register operates in locked mode. When S1=0 and S0=1, the data get shifted to right. When S1=1 and S0=0, mode the data gets shifted to left. When S1=1 and S0=1, the data gets shifted in parallel.The block diagram of the universal shift register is shown in Fig 9 and implementation of universal shift register using DETFF and PIPE logic is shown in Fig 10 and Fig 11.

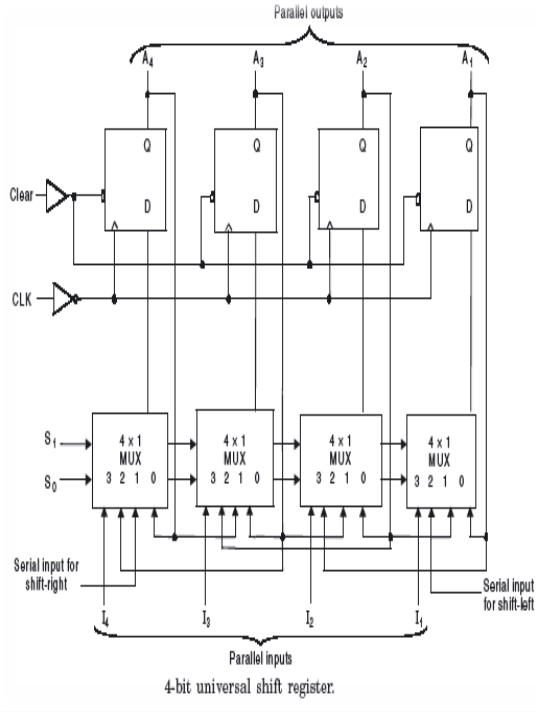


Fig.9 Block diagram of universal shift register

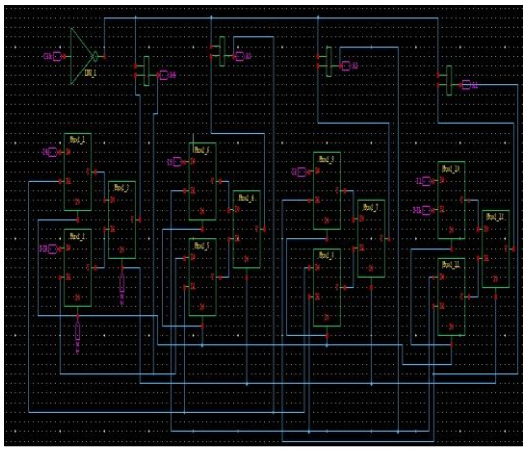

Fig.10 Design of Universal Shift Register Using DETFF

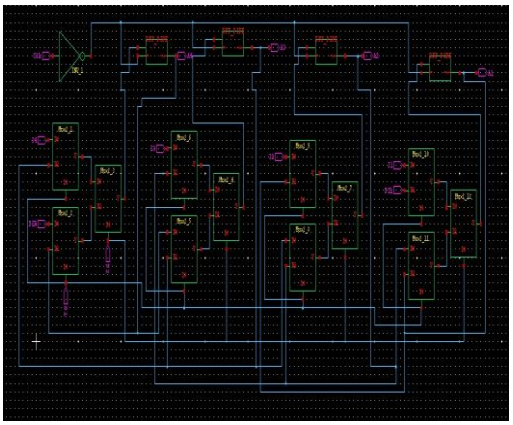

Fig.11 Design of Universal Shift Register Using PIPE logic

## VI. SIMULATION AND PERFORMANCE COMPARISON

To evaluate the performance, the universal shift registers are designed using two different flip-flop structures discussed in this paper is designed using 180-nm CMOS technology. All simulations are carried out using W-edit simulation tool with different range of frequencies from 100 MHz to 500MHz. The simulated waveform of the proposed modified pipe logic flip flop is shown in Fig.12

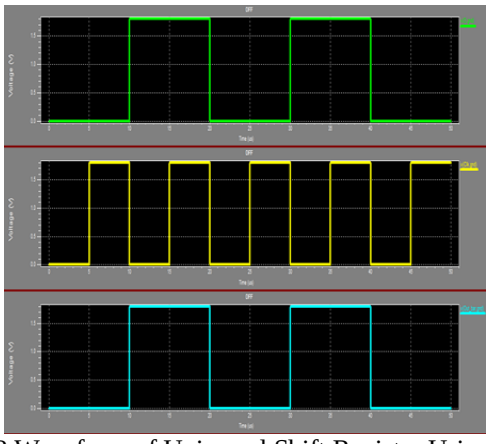

Fig.12 Waveform of Universal Shift Register Using PIPE logic


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In the performance comparison Table II represent the comparison of proposed flip flop using PIPE logic with other existing flip flops at a clock frequency of 100 KHz. The performance of the proposed Universal Shift Register Using PIPE logic is evaluated by comparing the power and power delay product (PDP) which is shown in the Table III as follows.

TABLE III: COMPARISON OF PROPOSED FLIP FLOP USING PIPE LOGIC WITH OTHER EXISTING FLIP FLOPS AT A CLOCK FREQUENCY OF 500 MHZ.

| Technology | Total Number Of Transistors Used | Total No Of Clocked Transistors | Average Power Consumption (µw) | Power Delay Product (aJ) | Area (µm²) |
|---|---|---|---|---|---|
| CDMFF | 20 | 5 | 46.62 | 58.4 | 12.5 |
| CPSFF | 15 | 3 | 42.38 | 46.2 | 9.37 |
| DETFF | 18 | 3 | 34.23 | 49.26 | 11.2 |
| MTCMOS | 18 | 3 | 39.84 | 41.54 | 11.2 |
| SCCER | 17 | 3 | 41.23 | 36.53 | 10.6 |
| **Proposed Flip Flop Using Pipe Logic** | **10** | **2** | **24.26** | **26.2** | **6.25** |

TABLE IIIII: COMPARISON OF UNIVERSAL SHIFT REGISTER USING DETFF WITH THE PROPOSED UNIVERSAL SHIFT REGISTER USING PIPE LOGIC AT VARIOUS CLOCK FREQUENCIES.

| **Clock frequency** | **Design Of Universal Shift Register using DETFF** | |
|---|---|---|
| | **Average power Consumption (µw)** | **Power delay product (aJ)** |
| 100Mhz | 127.1 | 65.23 |
| 500Mhz | 164.83 | 73.69 |
| **Clock frequency** | **Design Of Proposed Universal Shift Register Using Pipe Logic** | |
| | **Average power Consumption (µw)** | **Power delay product (aJ)** |
| 100Mhz | 87.65 | 46.55 |
| 500Mhz | 110.54 | 54.23 |

## VII. CONCLUSION

In this paper we have designed a low power and area efficient universal shift register using PIPE logic flip flop which is simulated using tanner tool at 180nm technology. We have made a performance comparison of the proposed flip flop using PIPE logic with various other flip flops. The proposed flip flop is having less number of transistors than the other flip-flops. Among those flip flops the best two flop flops are selected for designing the universal shift register. Universal shift register using DETFF and universal shift register with the flip flop using pipe logic are designed and their performances are compared with various clock frequencies. Further, the average power and the Power delay Product are improved by 33% and 27% when compared with existing design respectively. Therefore the proposed design has lower average power and lowest PDP than existing designs. Therefore the proposed design is well suited for low power and high performance applications.

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